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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,273	04/12/2001	Hunt Hang Jiang	6136/53945(25916-194)	4925

7590 03/06/2003

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EXAMINER	
MITCHELL, JAMES M	
ART UNIT	PAPER NUMBER
2827	#10

DATE MAILED: 03/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/834,273	JIANG ET AL.	
	Examiner	Art Unit	
	James Mitchell	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *11* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 16 is objected to because of the following informalities: there appears to be a grammatical error in the phrase "...layer terminates..." Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claim 1-20 and 28-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jimarez et al (U.S 6,225,206) in combination with Oxman (US 2002/0066528) and Agarwala et al (US 5,130,779).

5. Jimarez discloses (Fig 1-7) an article, apparatus and method comprising forming a dielectric layer on a circuitized substrate having conductive regions (16) that was inherently part of a wafer, disposing a first solder bump (14) that's generally dome on the conductive regions, laminating a photoimageable dielectric layer (18; Column 5, Line 28) to the circuitized substrate and on the first solder bump, and removing (opening) a portion dielectric layer and solder ball to expose a portion of the first solder bump that comprises an internal planar surface, and depositing a second solder bump (44) on the first solder bump., wherein inherently the first and second solder bumps are of inherently different solder compositions (Column 6, Lines 10-11) and the first solder has a reflow temperature greater than the reflow of the second solder (Col. 5, Lines 15-20); said first bump is generally dome shaped surface (shown in Fig 1) below a top surface of the dielectric layer, and where the dome partly protrudes above said top surface of the dielectric layer (shown in Fig 2) at a defined distance therefrom; and inherent circuitized substrate (via substrate, 12, 42 with pad); and an internal surface (Fig 4, via top surface of ball in contact with dielectric) of solder bump (14) disposed below a top surface of said dielectric layer at a defined distance.

6. Jimarez does not appear to disclose removing the dielectric layer through abrading or forming a barrier layer between the first and second solder bump with a thickness generally equal to said defined distance or between .01 to about 50% of the value of the thickness of the dielectric layer.

7. With respect to abrading, Jimarez discloses the same invention as applicant including except that the opening in the dielectric is made through ablating instead of abrading.

8. Oxman shows that ablating and abrading are equivalent processes known in the art known in the art (Lft. Col. Page 6, Lines 5-7). Therefore, because these removing processes are art recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute an ablating process with an abrading process thereby leaving a solder bump with an abraded internal planar surface.

9. Agarwala utilizes a barrier (Column 5, Lined 56-57) comprising a thickness and having a value generally equal to a defined distance and formed between solder bumps, wherein said barrier comprises a Group VIIIB, Fe covered by a layer of nobel metal, Nickel (Column 6, Line 35) and therefore coated, second solder terminates at a juncture point.

10. It would have been obvious to one of ordinary skill in the art to form the barrier of Agarwala on the internal dome, planar surface between the first and second solder bump of Jimarez in order to eliminate intersolder diffusion as taught by Agarwala (Column 5, lines 56-61).

11. With respect to claims 8, 9, 35 and 36 the thickness of the barrier layer, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an

unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

12. With respect claims 19, 28 and 29, neither Jimarez, Oxman or Agarwala appear to explicitly teach the process limitations of "coating...produced in accordance with the method of a claim...surface abraded;" however the product of Jimarez, Oxman or Agarwala inherently possesses the structural characteristics imparted by the process limitation. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

13. Claims 21-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jimarez et al, Oxman and Agarwala et al as applied to claim 20 and further combination with Yoshikazu (US 5,989,982).

14. Jimarez (Fig 4) further discloses an internal surface disposed below a top surface of said dielectric layer at a defined distance, but does not appear to disclose that the substrate is a wafer or that the thickness of a barrier layer is equal to said distance, however Yoshikau utilizes a substrate that is a wafer.

15. It would have been obvious to one of ordinary skill in the art to form the substrate of Jimarez as a wafer, in order to provide easier manufacture and chip package as taught by Yoshikazu (Abstract).

16. With respect to claim 22, see paragraph 8.

With respect to claim 26, see paragraph 11

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmm
March 4, 2003

DAVID E. G
PRIMARY EX